

### **REMARKS**

Claims 1, 3-5, 7, 8, 10-14, 16-19, 21, 23, 24, 26, 27, and 29-33 are pending in this application. Favorable reconsideration and allowance of the pending claims are respectfully requested.

#### **Examiner Interview**

Applicant would like to thank Examiner Mattis for conducting a telephone interview with Applicant's representative on August 24, 2007 to discuss the current grounds of rejection and the applied references. The substance of the interview is reflected below.

#### **Claim Rejections – 35 U.S.C. § 103(a)**

Claims 1, 3-5, 7, 8, 11-14, and 16-19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over United States Patent Number (USPN) 5,410,540 to Aiki et al. ("Aiki") in view of USPN 6,751,219 to Lipp et al ("Lipp") and USPN 6,574,194 to Sun et al. ("Sun").

Claim 10 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Aiki in view of Lipp and Sun and in further view of United States Patent Application Publication Number 2005/0041579 to Medina et al ("Medina").

Claims 21, 23, 24, 26, 27, and 29-33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Aiki in view of Lipp, Sun, and USPN 6,724,761 to Moy-Yee et al ("Moy-Yee").

Applicant respectfully traverses these rejections.

In response to the previous Office Action, Independent claim 1 was amended to recite, among its other elements, “a first memory comprising multiple segments, each segment comprising multiple independently addressable channels, the first logic circuit configured to determine a number of channels and segments needed to store the number of copies of the input data frame, the first memory coupled to the first logic circuit and configured to store multiple copies of the input data frame within a single segment of the determined number of segments and to read the multiple copies of the input data frame from the single segment in a single read cycle.”

Independent claim 14 was amended to recite, among its other elements, “a memory coupled to the first logic circuit and configured to store and read the copies of the input data frame, the memory being comprised of segments including independently addressable channels with one or more segments being accessible at a given time, the first logic circuit configured to determine a number of channels and segments needed to store the number of copies of the input data frame, the first memory to store multiple copies of the input data frame within a single segment of the determined number of segments and to read the multiple copies of the input data frame from the single segment in a single read cycle.”

Independent claim 21 was amended to recite, among its other elements, “memory comprising multiple segments, each segment comprising multiple independently addressable channels; a processor coupled to the memory and programmed to determine the number of copies of the input data frame to make and to determine when to read at least one copy of the input data frame from the memory, the processor configured to determine a number of channels and segments needed to store the number of copies of

the input data frame, the memory to store multiple copies of the input data frame within a single segment of the determined number of segments and to read the multiple copies of the input data frame from the single segment in a single read cycle.”

Independent claim 29 was amended to recite, among its other elements, “determine a number of channels and segments needed to store the number of copies of the input data frame; forward instructions and the copies of the received data frame to the memory so as to cause the memory to store multiple copies of the received data frame within a single segment of the determined number of segments; forward instructions to the memory to read out the multiple copies of the received data frame from the single segment in parallel and output the copies onto a bus in a single clock cycle.”

Applicant submits that none of the cited references including Aiki, Lipp, Sun, Medina, and Moy-Yee teaches or suggests the above features as recited in amended independent claims 1, 14, 21, and 29. In particular, Applicant notes that the claimed features of storing multiple copies of the input data frame within a single segment of the determined number of segments and reading the multiple copies of the input data frame from the single segment in a single read cycle were not addressed in the Final Office Action.

Additionally, even if the cited references could be combined, which Applicant does not admit, such combination would fail to teach or suggest all of the features of amended independent claims 1, 14, 21, and 29. Therefore, the cited references, whether alone or in combination, are insufficient to render obvious the subject matter of independent claims 1, 14, 21, and 29. Accordingly, Applicant respectfully requests withdrawal of the rejection and allowance of the pending claims.

As discussed in the Examiner Interview, the prior amendments to the independent claims are clearly supported by exemplary portions of the Specification and the accompanying Figures as follows.

“An exemplary main memory 125 may have four channels, each of which is 64 bytes wide, and sixteen segments. This means that main memory 125 and store 64, 64-byte data frames (one in each channel in each segment), sixteen 256-byte data frames (one spanning all four channels in each segment), or other combinations. (Specification at page 9, line 20 - page 10, line 2). When a data frame is received, a determination is made as to which portion of main memory 125 is to store the received data frame. (Specification at page 10, lines 12-14). Since main memory 125 is divided into discrete channels, a determination is needed as to how many channels are required to store one copy of the received data frame.” (Specification at page 11, lines 19-21).

“Channel availability circuit 610 receives the outputs from memory 305 and determines where there are vacant channels...The results are output to segment availability circuit 615 and arbitrator circuit 620. Depending on the design of channel availability circuit 610, it may only register availability in contiguous channels and he segment are vacant or it may register availability if the proper number of channels is available regardless of contiguousness.” (Specification at page 13, lines 3-14).

“Once all of the suitable locations in frame memory and have been identified, one or more locations are selected to store the copies of the data frame (step 835). The copies of the data frame are then stored in selected memory locations of the frame memory (step 840).” (Specification at page 16, lines 3-9).

“As shown in Fig. 10a, four data frames, each only a single channel wide, are stored in a segment 1005 of main memory in a conventional switch. The data frames are forwarded to copier 1010 where the necessary copies are made. In this example, two copies of each data frame are generated before the data frames are output to the ports. Since copier 1010 can only copy one data frame at a time, it follows that four read cycles are needed to output the four data frames L-O from Segment 9. It should be noted that if copier circuit 1010 were not present, the number of read cycles to output the four data frames shown increases to eight. It should also be noted that if multiple data frames are not packed into a single segment, the use of memory would be less efficient.”  
(Specification at page 17, line 14 - page 18, line 2).

“In contrast, Fig. 10b, shows to segments 1015 and 1020, which have multiple copies of data frames already in them, in accordance with the implementations described above. Due to the packing up all of the needed copies of the data frames into a single segment, the implementations described above will output the required L and M data frames in one read cycle and the N and O data frames in another cycle. Assuming that there are no port collisions such as the L data frame and the M data frame being transmitted over the same port, the implementations described can transmit the needed data frames in half the time of conventional switches (i.e., in two read cycles).”

In view of the above, Applicant submits that claims 1, 3-5, 7, 8, 10-14, 16-19, 21, 23, 24, 26, 27, and 29-33 recite novel features not shown by the cited references. Furthermore, Applicant submits that claims 1, 3-5, 7, 8, 10-14, 16-19, 21, 23, 24, 26, 27, and 29-33 are non-obvious and represent patentable subject matter in view of the cited references, whether taken alone or in combination. Accordingly, Applicant submits that

the claims 1, 3-5, 7, 8, 10-14, 16-19, 21, 23, 24, 26, 27, and 29-33 are not anticipated nor rendered obvious in view of the cited references. Moreover, Applicant submits that the above-recited novel features provide new and unexpected results not recognized by the cited references. Therefore, Applicant respectfully requests reconsideration and withdrawal of the § 103(a) rejections.

Applicant does not otherwise concede, however, the correctness of the Office Action's rejection with respect to any of the dependent claims discussed above. Accordingly, Applicant hereby reserves the right to make additional arguments as may be necessary to further distinguish the dependent claims from the cited references, taken alone or in combination, based on additional features contained in the dependent claims that were not discussed above. A detailed discussion of these differences is believed to be unnecessary at this time in view of the basic differences in the independent claims pointed out above.

It is believed that claims 1, 3-5, 7, 8, 10-14, 16-19, 21, 23, 24, 26, 27, and 29-33 are in allowable form. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17.

Respectfully submitted,

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Under 37 CFR 1.34(a)

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